

Bias Resistor Transistor

PNP Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

LDTBG12GPLT1G

●Applications

Driver

●Features

- 1) High h_{FE} .
300 (Min.) ($V_{CE} / I_C = 2V / 0.5A$)
 - 2) Low saturation voltage,
($V_{CE(sat)} = 0.4V$ at $I_C / I_B = 500mA / 5mA$)
 - 3) Built-in zener diode gives strong protection against reverse surge by L- load (an inductive load).
- We declare that the material of product compliance with RoHS requirements.

●Structure

 PNP epitaxial planar silicon transistor
(with built-in resistor and zener diode)

●Absolute maximum ratings ($T_a = 25^\circ C$)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V_{CBO}	-60 ± 10	V
Collector-emitter voltage	V_{CEO}	-60 ± 10	V
Emitter-base voltage	V_{EBO}	-5	V
Collector current	I_C	-1	A
	I_{CP}	-2 *1	A
Collector power dissipation	P_C	0.5	W
		2 *2	
Junction temperature	T_j	150	$^\circ C$
Storage temperature	T_{stg}	-55 to $+150$	$^\circ C$

 *1 $P_w \leq 10ms$, Duty cycle $\leq 1/2$

 *2 When mounted on a $40 \times 40 \times 0.7$ mm ceramic board.

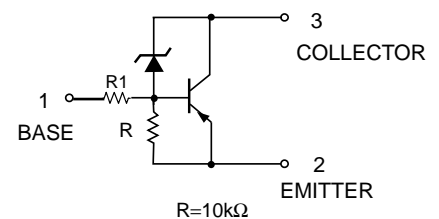
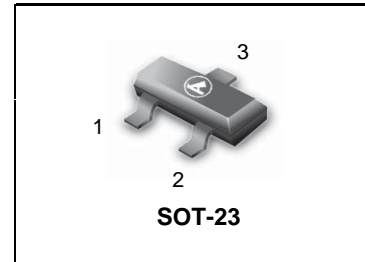
DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Shipping
LDTBG12GPLT1G	Q8	1	22	3000/Tape & Reel
LDTBG12GPLT3G	Q8	1	22	10000/Tape & Reel

●Electrical characteristics ($T_a = 25^\circ C$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	-50	-	-70	V	$I_C = -50\mu A$
Collector-emitter breakdown voltage	BV_{CEO}	-50	-	-70	V	$I_C = -1mA$
Emitter-base breakdown voltage	BV_{EBO}	-5	-	-	V	$I_E = -720\mu A$
Collector cutoff current	I_{CBO}	-	-	-0.5	μA	$V_{CB} = -40V$
Emitter cutoff current	I_{EBO}	-300	-	-580	μA	$V_{EB} = -4V$
Collector-emitter saturation voltage	$V_{CE(sat)}$	-	-	-0.4	V	$I_C / I_B = -500mA / -5mA$
DC current transfer ratio	h_{FE}	300	-	-	-	$V_{CE} = -2V, I_C = -500mA$
Emitter-base resistance	R	7	10	13	$k\Omega$	-
Transition frequency	f_t *	-	80	-	MHz	$V_{CE} = -5V, I_E = -0.1A, f = -30MHz$

* Characteristics of built-in transistor



LDTBG12GPLT1G

●Electrical characteristic curves

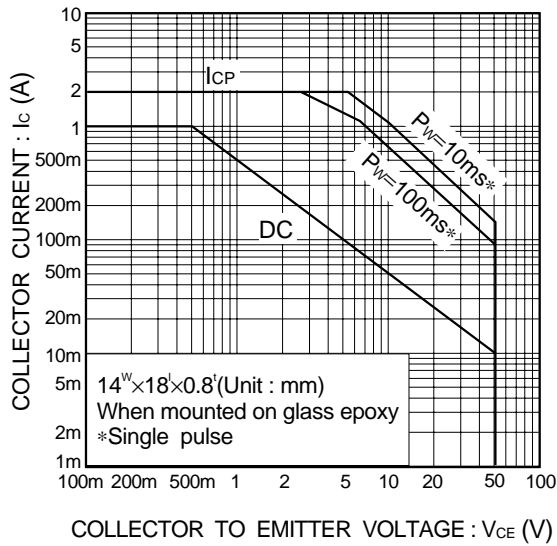


Fig.1 Safe operating area

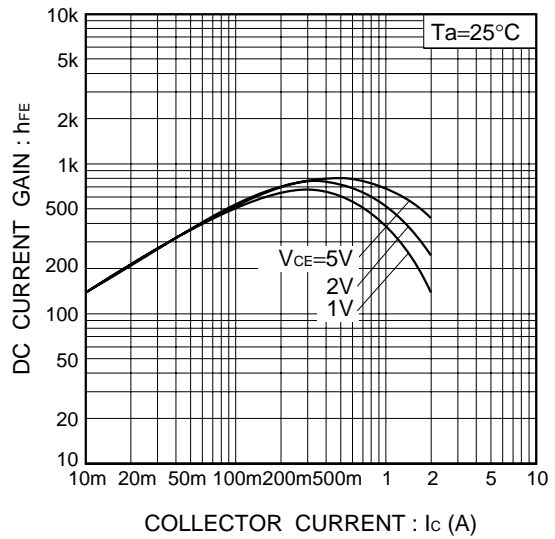


Fig.2 DC current gain vs. collector current

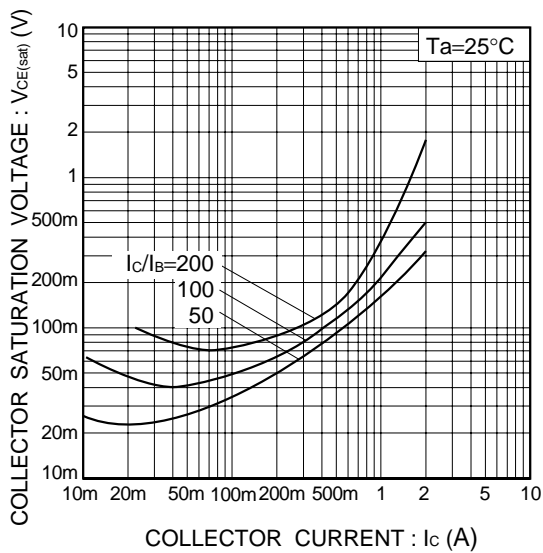


Fig.3 Collector-emitter saturation voltage vs. collector current

