

SiT9120

Standard Frequency Differential Oscillator



Features

- 31 standard frequencies from 25 MHz to 212.5 MHz
- LVPECL and LVDS output signaling types
- 0.6 ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- Frequency stability as low as ± 10 ppm
- Industrial and extended commercial temperature ranges
- Industry-standard packages: 3.2x2.5, 5.0x3.2 and 7.0x5.0 mmxmm
- For any other frequencies between 1 to 625 MHz, refer to SiT9121 and SiT9122 datasheet

Applications

- 10GB Ethernet, SONET, SATA, SAS, Fibre Channel, PCI-Express
- Telecom, networking, instrumentation, storage, servers



Electrical Characteristics

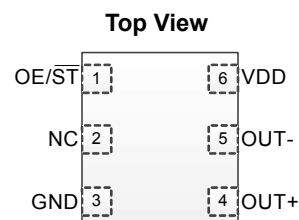
| Parameter and Conditions | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---------------------------------|----------------------|------|----------------------|-----------------|--|
| LVPECL and LVDS, Common Electrical Characteristics | | | | | | |
| Supply Voltage | V _{dd} | 2.97 | 3.3 | 3.63 | V | |
| | | 2.25 | 2.5 | 2.75 | V | |
| | | 2.25 | – | 3.63 | V | Termination schemes in Figures 1 and 2 - XX ordering code |
| Output Frequency Range | f | 25 | – | 212.5 | MHz | See last page for list of standard frequencies |
| Frequency Stability | F _{stab} | -10 | – | +10 | ppm | Inclusive of initial tolerance, operating temperature, rated power supply voltage, and load variations |
| | | -20 | – | +20 | ppm | |
| | | -25 | – | +25 | ppm | |
| | | -50 | – | +50 | ppm | |
| First Year Aging | F _{aging1} | -2 | – | +2 | ppm | 25°C |
| 10-year Aging | F _{aging10} | -5 | – | +5 | ppm | 25°C |
| Operating Temperature Range | T _{use} | -40 | – | +85 | °C | Industrial |
| | | -20 | – | +70 | °C | Extended Commercial |
| Input Voltage High | V _{IH} | 70% | – | – | V _{dd} | Pin 1, OE or \overline{ST} |
| Input Voltage Low | V _{IL} | – | – | 30% | V _{dd} | Pin 1, OE or \overline{ST} |
| Input Pull-up Impedance | Z _{in} | – | 100 | 250 | k Ω | Pin 1, OE logic high or logic low, or \overline{ST} logic high |
| | | 2 | – | – | M Ω | Pin 1, \overline{ST} logic low |
| Start-up Time | T _{start} | – | 6 | 10 | ms | Measured from the time V _{dd} reaches its rated minimum value. |
| Resume Time | T _{resume} | – | 6 | 10 | ms | In Standby mode, measured from the time \overline{ST} pin crosses 50% threshold. |
| Duty Cycle | DC | 45 | – | 55 | % | Contact SiTime for tighter duty cycle |
| LVPECL, DC and AC Characteristics | | | | | | |
| Current Consumption | I _{dd} | – | 61 | 69 | mA | Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V |
| OE Disable Supply Current | I _{OE} | – | – | 35 | mA | OE = Low |
| Output Disable Leakage Current | I _{leak} | – | – | 1 | μ A | OE = Low |
| Standby Current | I _{std} | – | – | 100 | μ A | \overline{ST} = Low, for all V _{dds} |
| Maximum Output Current | I _{driver} | – | – | 30 | mA | Maximum average current drawn from OUT+ or OUT- |
| Output High Voltage | V _{OH} | V _{dd} -1.1 | – | V _{dd} -0.7 | V | See Figure 1(a) |
| Output Low Voltage | V _{OL} | V _{dd} -1.9 | – | V _{dd} -1.5 | V | See Figure 1(a) |
| Output Differential Voltage Swing | V _{Swing} | 1.2 | 1.6 | 2.0 | V | See Figure 1(b) |
| Rise/Fall Time | T _r , T _f | – | 300 | 500 | ps | 20% to 80%, see Figure 1(a) |
| OE Enable/Disable Time | T _{oe} | – | – | 115 | ns | f = 212.5 MHz - For other frequencies, T _{oe} = 100ns + 3 period |
| RMS Period Jitter | T _{jitt} | – | 1.2 | 1.7 | ps | f = 100 MHz, V _{DD} = 3.3V or 2.5V |
| | | – | 1.2 | 1.7 | ps | f = 156.25 MHz, V _{DD} = 3.3V or 2.5V |
| | | – | 1.2 | 1.7 | ps | f = 212.5 MHz, V _{DD} = 3.3V or 2.5V |
| RMS Phase Jitter (random) | T _{phj} | – | 0.6 | 0.85 | ps | f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dds} |
| LVDS, DC and AC Characteristics | | | | | | |
| Current Consumption | I _{dd} | – | 47 | 55 | mA | Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V |
| OE Disable Supply Current | I _{OE} | – | – | 35 | mA | OE = Low |
| Differential Output Voltage | V _{OD} | 250 | 350 | 450 | mV | See Figure 2 |

Electrical Characteristics (continued)

| Parameter and Conditions | Symbol | Min. | Typ. | Max. | Unit | Condition |
|--|---------------------------------|-------|------|-------|------|--|
| LVDS, DC and AC Characteristics (continued) | | | | | | |
| Output Disable Leakage Current | I _{leak} | – | – | 1 | μA | OE = Low |
| Standby Current | I _{std} | – | – | 100 | μA | \overline{ST} = Low, for all V _{dds} |
| VOD Magnitude Change | ΔVOD | – | – | 50 | mV | See Figure 2 |
| Offset Voltage | VOS | 1.125 | 1.2 | 1.375 | V | See Figure 2 |
| VOS Magnitude Change | ΔVOS | – | – | 50 | mV | See Figure 2 |
| Rise/Fall Time | T _r , T _f | – | 495 | 600 | ps | 20% to 80%, see Figure 2 |
| OE Enable/Disable Time | T _{oe} | – | – | 115 | ns | f = 212.5 MHz - For other frequencies, T _{oe} = 100ns + 3 period |
| RMS Period Jitter | T _{jitt} | – | 1.2 | 1.7 | ps | f = 100 MHz, VDD = 3.3V or 2.5V |
| | | – | 1.2 | 1.7 | ps | f = 156.25 MHz, VDD = 3.3V or 2.5V |
| | | – | 1.2 | 1.7 | ps | f = 212.5 MHz, VDD = 3.3V or 2.5V |
| RMS Phase Jitter (random) | T _{phj} | – | 0.6 | 0.85 | ps | f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dds} |

Pin Description

| Pin | Map | | Functionality |
|-----|-----------------|--------|---|
| 1 | OE | Input | H or Open: specified frequency output L: output is high impedance |
| | \overline{ST} | Input | H or Open: specified frequency output L: Device goes to sleep mode. Supply current reduces to I _{std} . |
| 2 | NC | NA | No Connect; Leave it floating or connect to GND for better heat dissipation |
| 3 | GND | Power | VDD Power Supply Ground |
| 4 | OUT+ | Output | Oscillator output |
| 5 | OUT- | Output | Complementary oscillator output |
| 6 | VDD | Power | Power supply voltage |



Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Min. | Max. | Unit |
|--|------|------|------|
| Storage Temperature | -65 | 150 | °C |
| VDD | -0.5 | 4 | V |
| Electrostatic Discharge (HBM) | – | 2000 | V |
| Soldering Temperature (follow standard Pb free soldering guidelines) | – | 260 | °C |

Thermal Consideration

| Package | θJA, 4 Layer Board (°C/W) | θJC, Bottom (°C/W) |
|-------------|---------------------------|--------------------|
| 7050, 6-pin | 38.1 | 26.9 |
| 5032, 6-pin | 68.1 | 17.5 |
| 3225, 6-pin | 97.4 | 15.2 |

Environmental Compliance

| Parameter | Condition/Test Method |
|----------------------------|---------------------------|
| Mechanical Shock | MIL-STD-883F, Method 2002 |
| Mechanical Vibration | MIL-STD-883F, Method 2007 |
| Temperature Cycle | JESD22, Method A104 |
| Solderability | MIL-STD-883F, Method 2003 |
| Moisture Sensitivity Level | MSL1 @ 260°C |

Waveform Diagrams

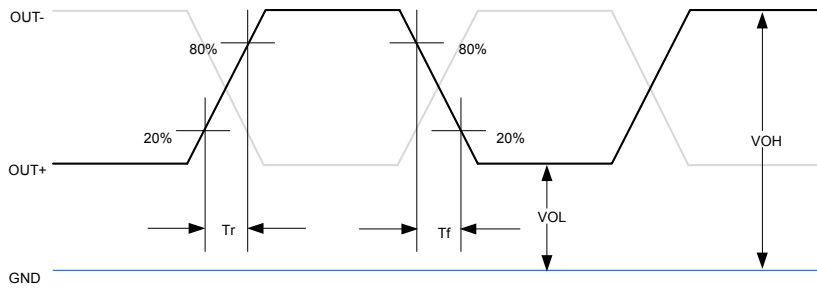


Figure 1(a). LVPECL Voltage Levels per Differential Pin (OUT+/OUT-)

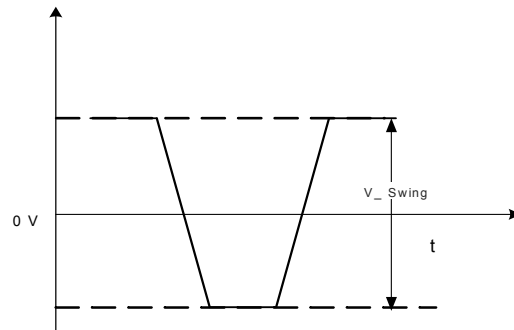


Figure 1(b). LVPECL Voltage Levels Across Differential Pair

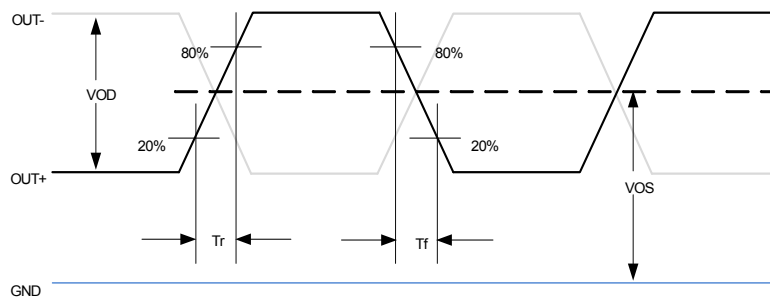


Figure 2. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

Termination Diagrams

LVPECL:

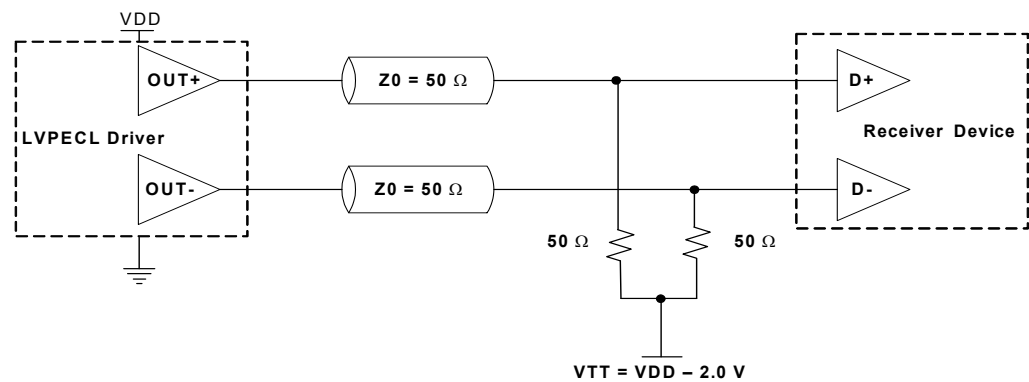


Figure 3. LVPECL Typical Termination

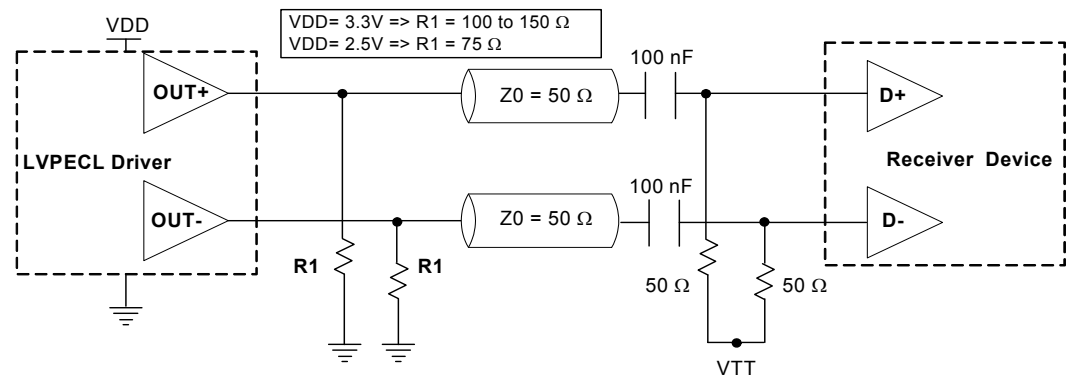


Figure 4. LVPECL AC Coupled Termination

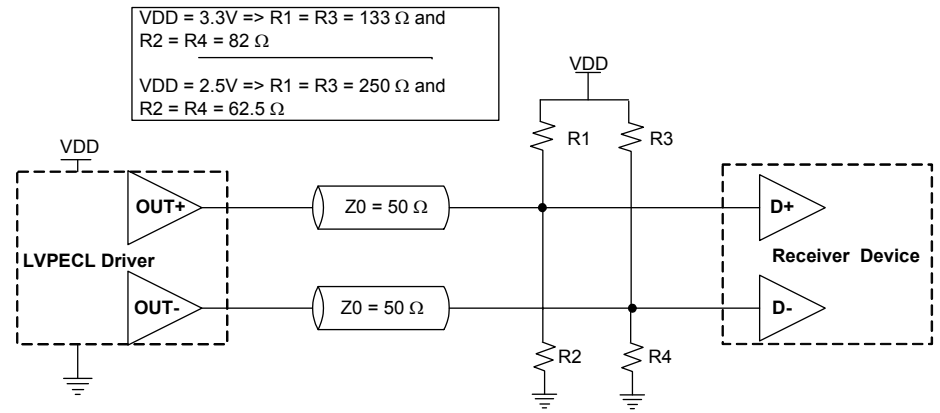


Figure 5. LVPECL with Thevenin Typical Termination

LVDS:

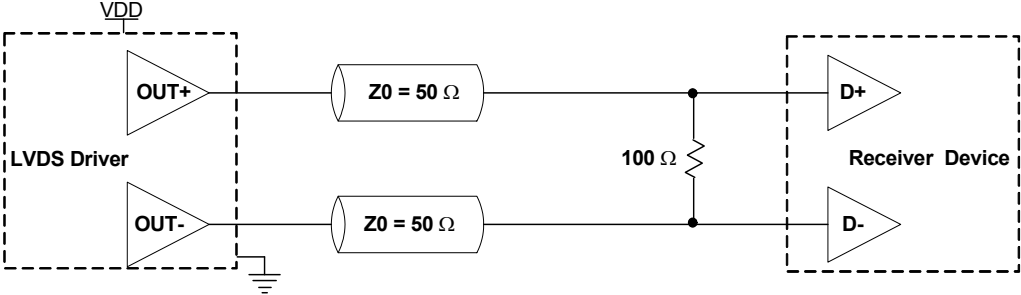
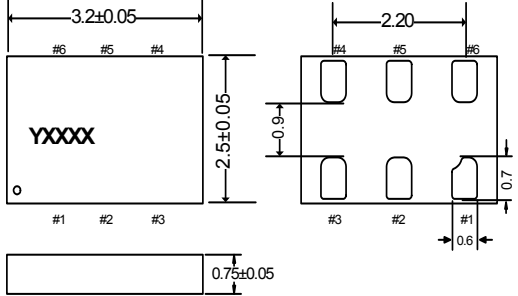
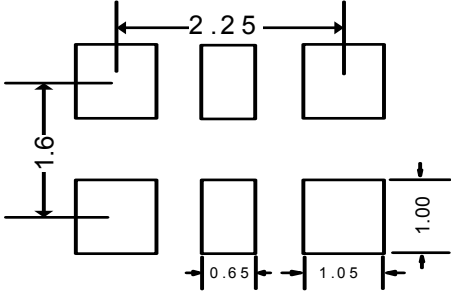
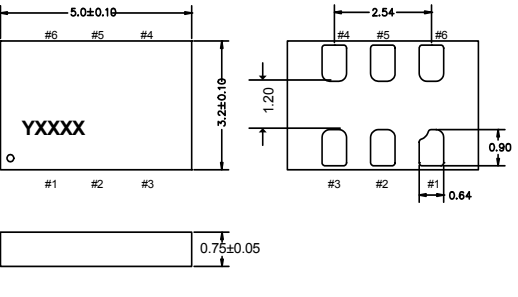
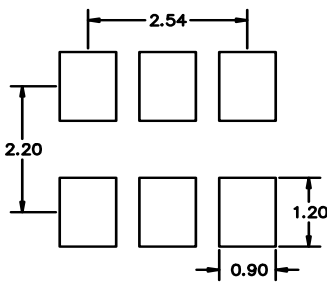
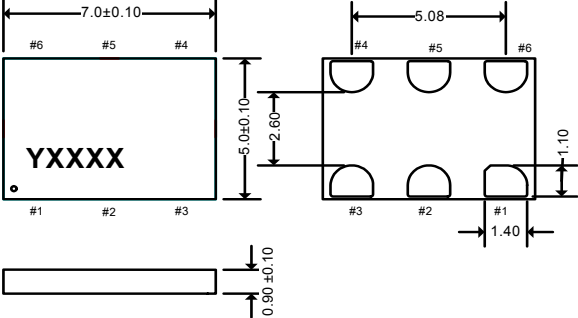
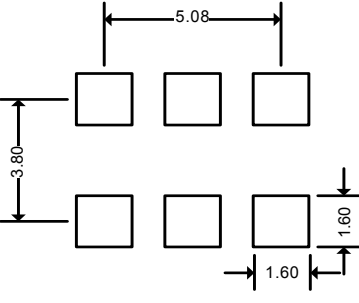


Figure 6. LVDS Single Termination (Load Terminated)

Dimensions and Patterns

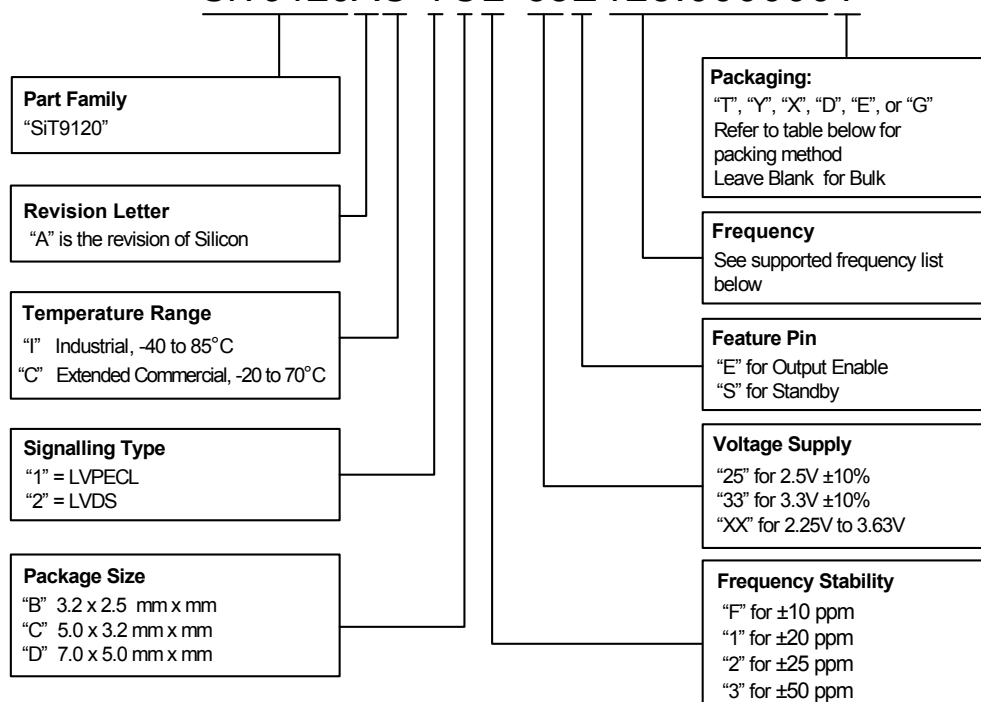
| Package Size – Dimensions (Unit: mm) ^[1] | Recommended Land Pattern (Unit: mm) ^[2] |
|--|--|
| <p>3.2 x 2.5x 0.75 mm</p>  |  |
| <p>5.0 x 3.2 x 0.75 mm</p>  |  |
| <p>7.0 x 5.0x 0.90 mm</p>  |  |

Notes:

1. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
2. A capacitor of value 0.1 μ F between Vdd and GND is recommended.

Ordering Information

SiT9120AC-1C2-33E 125.000000T



Supported Frequencies

| | | | | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| 25.000000 MHz | 50.000000 MHz | 74.175824 MHz | 74.250000 MHz | 75.000000 MHz | 98.304000 MHz | 100.000000 MHz | 106.250000 MHz |
| 125.000000 MHz | 133.000000 MHz | 133.300000 MHz | 133.330000 MHz | 133.333000 MHz | 133.333300 MHz | 133.333330 MHz | 133.333333 MHz |
| 148.351648 MHz | 148.500000 MHz | 150.000000 MHz | 155.520000 MHz | 156.250000 MHz | 161.132800 MHz | 166.000000 MHz | 166.600000 MHz |
| 166.660000 MHz | 166.666000 MHz | 166.666600 MHz | 166.666660 MHz | 166.666666 MHz | 200.000000 MHz | 212.500000 MHz | |

Ordering Codes for Supported Tape & Reel Packing Method

| Device Size | 8 mm T&R (3ku) | 8 mm T&R (1ku) | 8 mm T&R (250u) | 12 mm T&R (3ku) | 12 mm T&R (1ku) | 12 mm T&R (250u) | 16 mm T&R (3ku) | 16 mm T&R (1ku) | 16 mm T&R (250u) |
|--------------|----------------|----------------|-----------------|-----------------|-----------------|------------------|-----------------|-----------------|------------------|
| 7.0 x 5.0 mm | - | - | - | - | - | - | T | Y | X |
| 5.0 x 3.2 mm | - | - | - | T | Y | X | - | - | - |
| 3.2 x 2.5 mm | D | E | G | T | Y | X | - | - | - |

Revision History

| Version | Release Date | Change Summary |
|---------|--------------|--|
| 1.01 | 2/20/13 | Original |
| 1.02 | 11/23/13 | Added input specifications, LVPECL/LVDS waveforms, packaging T&R options |
| 1.03 | 2/6/14 | Added 8mm T&R option |
| 1.04 | 3/3/14 | Added ± 10 ppm |
| 1.05 | 7/23/14 | Include Thermal Consideration Table |

© SiTime Corporation 2014. The information contained herein is subject to change at any time without notice. SiTime assumes no responsibility or liability for any loss, damage or defect of a Product which is caused in whole or in part by (i) use of any circuitry other than circuitry embodied in a SiTime product, (ii) misuse or abuse including static discharge, neglect or accident, (iii) unauthorized modification or repairs which have been soldered or altered during assembly and are not capable of being tested by SiTime under its normal test conditions, or (iv) improper installation, storage, handling, warehousing or transportation, or (v) being subjected to unusual physical, thermal, or electrical stress.

Disclaimer: SiTime makes no warranty of any kind, express or implied, with regard to this material, and specifically disclaims any and all express or implied warranties, either in fact or by operation of law, statutory or otherwise, including the implied warranties of merchantability and fitness for use or a particular purpose, and any implied warranty arising from course of dealing or usage of trade, as well as any common-law duties relating to accuracy or lack of negligence, with respect to this material, any SiTime product and any product documentation. Products sold by SiTime are not suitable or intended to be used in a life support application or component, to operate nuclear facilities, or in other mission critical applications where human life may be involved or at stake. All sales are made conditioned upon compliance with the critical uses policy set forth below.

CRITICAL USE EXCLUSION POLICY
BUYER AGREES NOT TO USE SITIME'S PRODUCTS FOR ANY APPLICATION OR IN ANY COMPONENTS USED IN LIFE SUPPORT DEVICES OR TO OPERATE NUCLEAR FACILITIES OR FOR USE IN OTHER MISSION-CRITICAL APPLICATIONS OR COMPONENTS WHERE HUMAN LIFE OR PROPERTY MAY BE AT STAKE.

SiTime owns all rights, title and interest to the intellectual property related to SiTime's products, including any software, firmware, copyright, patent, or trademark. The sale of SiTime products does not convey or imply any license under patent or other rights. SiTime retains the copyright and trademark rights in all documents, catalogs and plans supplied pursuant to or ancillary to the sale of products or services by SiTime. Unless otherwise agreed to in writing by SiTime, any reproduction, modification, translation, compilation, or representation of this material shall be strictly prohibited.