



ELECTRICAL CHARACTERISTICS

For ESD protection - E series

Part Number	Working Voltage (Vw)	Breakdown Voltage (Vb)	Clamping Voltage (Vc)	Peak Current (Ip)	Transient Energy (Et)	Typical Capacitance (C)	
	Volt	Volt	Volt	Amp	Joule	pF	
	<50 μ A	1mA(DC)	1A,8/20 μ s	8/20 μ s	10/1000 μ s	1kHz	1MHz
JMV0402E200T220	12.0	15.0~25.0	50.0	1min.	0.05max.	-	22
JMV0402E270T150	17.0	21.6~32.4	66.0	1min.	0.05max.	-	15
JMV0402E270T300	17.0	21.6~32.4	66.0	1min.	0.05max.	-	30
JMV0402E520T030	17.0	41.6~56.0	130.0	1min.	0.05max.	-	3.0
JMV0603E270T150	17.0	21.6~32.4	66.0	2min.	0.05max.	-	15
JMV0603E270T300	17.0	21.6~32.4	66.0	2min.	0.05max.	-	30
JMV0603E520T030	17.0	41.6~56.0	130.0	2min.	0.05max.	-	3.0
JMV0603E620T150	17.0	55.8~68.2	120.0	2min.	0.05max.	-	15
JMV0603E620T300	17.0	55.8~68.2	120.0	2min.	0.05max.	-	30

Vw - The max. steady state DC operating voltage of which varistor could maintain also not exceeding 50 μ A leakage current.
 Vb - The voltage acrossed the devic measured at 1mA DC current.
 Vc - The peak voltage acrossed the varistor measured at a specified pulse current and waveform.
 Ip - The Minimum. peak current applied with specified waveform without any possibility of device fail.
 Et - The maximum. energy which dissipated with the specified waveform without any possibility of device fail.
 C - The device capacitance measured with zero volt bias , 1.0 Vrms and 1KHz / 0.5 Vrms and 1MHz.

For ESD Protection-Low capacitance Series

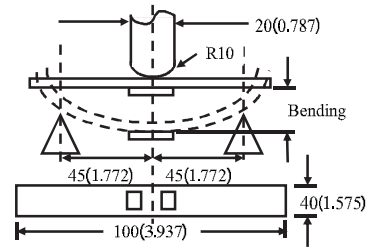
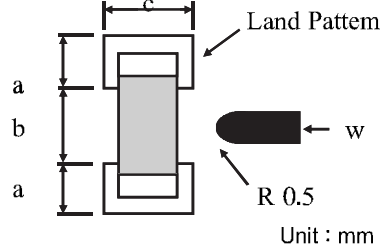
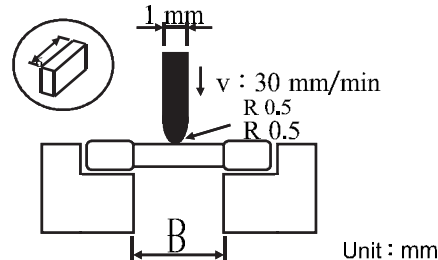
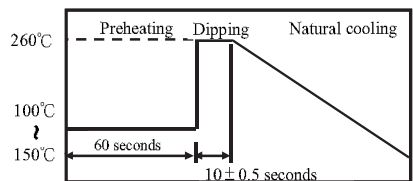
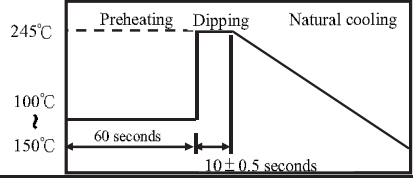
Part No.	Size (mm)	Vw	Trigger Voltage* (Vt)	Clamping Voltage* (Vc)	ESD		ESD Pulse Withstand* min.	Cp (1MHz, 1Vrms)
					Contact	Air		
JES0402C5R5T0R2	0402	5.5	500	35	8KV	15KV	500	0.2
JES0402C120T0R2		12						
JES0402C5R5T0R1		5.5						
JES0402C120T0R1		12						
JES0603C5R5T0R2	0603	5.5	500	35	8KV	15KV	500	0.2
JES0603C120T0R2		12						
JES0603C240T0R2		24						
JES0603C5R5T0R1		5.5						
JES0603C120T0R1		12						
JES0603C240T0R1		24						

* - Per IEC 61000-4-2, 8KV, Clamp measurement made 30ns after initiation of pulse, all test in contact discharge mode.
 Vw - The max. steady state DC operating voltage of which varistor could maintain also not exceeding 50 μ A leakage current.
 Vc - The peak voltage acrossed the varistor measured at a specified pulse current and waveform.
 C - The device capacitance measured with zero volt bias , 1MHz.

防靜電保護

JOYIN CO., LTD.
Metal Oxide Varistor

■ Reliability-Multilayer Chip Varistor

Test description	Standard	Performance	Test condition																																								
Board flexure strength	IEC60068-2-21	No mechanical damage shall be noticed even when the board is bent 2mm (0.079inches)	Solder a chip on a test substrate. Bend the substrat by 2mm(0.079in) 																																								
Flexure strength	Specification Standard	The terminal electrode and chip body must not be damaged by the forces applied. <table border="1" data-bbox="446 952 1029 1108"> <thead> <tr> <th>SIZE</th> <th>0402</th> <th>0603</th> <th>0805</th> <th>1206</th> <th>1210</th> <th>1812</th> <th>2220</th> </tr> </thead> <tbody> <tr> <td>a</td> <td>-</td> <td>1.0</td> <td>1.0</td> <td>1.3</td> <td>1.3</td> <td>1.5</td> <td>1.8</td> </tr> <tr> <td>b</td> <td>-</td> <td>0.8</td> <td>1.0</td> <td>1.5</td> <td>1.5</td> <td>3.6</td> <td>4.6</td> </tr> <tr> <td>c</td> <td>-</td> <td>1.3</td> <td>1.3</td> <td>3.0</td> <td>3.0</td> <td>3.8</td> <td>5.8</td> </tr> <tr> <td>w(kgf)</td> <td>-</td> <td>1.0</td> <td>4.0</td> <td>5.0</td> <td>5.0</td> <td>5.0</td> <td>5.0</td> </tr> </tbody> </table>	SIZE	0402	0603	0805	1206	1210	1812	2220	a	-	1.0	1.0	1.3	1.3	1.5	1.8	b	-	0.8	1.0	1.5	1.5	3.6	4.6	c	-	1.3	1.3	3.0	3.0	3.8	5.8	w(kgf)	-	1.0	4.0	5.0	5.0	5.0	5.0	 Unit : mm
SIZE	0402	0603	0805	1206	1210	1812	2220																																				
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b	-	0.8	1.0	1.5	1.5	3.6	4.6																																				
c	-	1.3	1.3	3.0	3.0	3.8	5.8																																				
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Bending strength	IEC60068-2-21	The ceramic chip shall not be damaged be the forces applied under the following conditions. <table border="1" data-bbox="446 1254 1029 1355"> <thead> <tr> <th>TYPE</th> <th>0402</th> <th>0603</th> <th>0805</th> <th>1206</th> <th>1210</th> <th>1812</th> <th>2220</th> </tr> </thead> <tbody> <tr> <td>D(mm)</td> <td>-</td> <td>1.3</td> <td>1.3</td> <td>2.0</td> <td>2.0</td> <td>3.8</td> <td>4.8</td> </tr> <tr> <td>W(kgf)</td> <td>-</td> <td>2.0</td> <td>3.0</td> <td>4.0</td> <td>4.0</td> <td>5.0</td> <td>5.0</td> </tr> </tbody> </table>	TYPE	0402	0603	0805	1206	1210	1812	2220	D(mm)	-	1.3	1.3	2.0	2.0	3.8	4.8	W(kgf)	-	2.0	3.0	4.0	4.0	5.0	5.0	 Unit : mm																
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Resistance to solder heat	IEC60068-2-20	The ceramic chip shall not be damaged. Shall be covered with solder. Vb: Within ±10% of the initial value.	Preheat:100°C~150°C,60seconds Solder temperature:260±5°C Dip time:10±1 seconds 																																								
Solderability	IEC60068-2-58	More than 90% of terminal electrode shall be covered with solder.	Preheat:100°C~150°C,60seconds Solder temperature:245±3°C Dip time:3±0,3seconds 																																								

防靜電保護

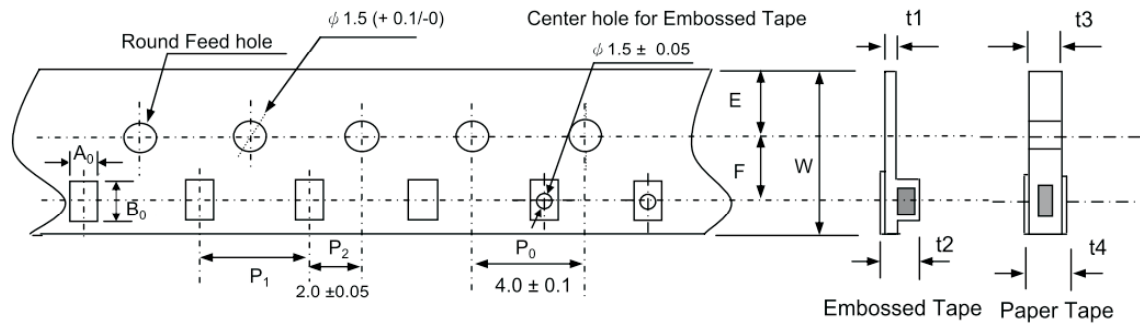


JOYIN CO., LTD.
Metal Oxide Varistor

■ Reliability-Multilayer Chip Varistor

Test description	Standard	Performance	Test condition
High temperature Load	IEC61051-1	Appearance:ceramic chip shall not be damaged. Vb:Within $\pm 10\%$ of the initial value	Temperature: $85 \pm 2^\circ\text{C}$ Testing time:1000 \pm 24hours Load Voltage:Working voltage Measurement : After placing for 24 hours min.
Damp Heat Load, Steady State	IEC60068-2-78	Appearance:ceramic chip shall not be damaged. Vb:Within $\pm 10\%$ of the initial value	Humidity:90 to 95% RH Temperature: $40 \pm 2^\circ\text{C}$ Testing time:500 \pm 24 hours at V_{DC} Measurement : After placing for 24 hours min.
Rapid Change of Temperature	IEC61051-1	Appearance:Cracking,chipping or any other defects harmful to the characteristics shall not be allowed Vb:Within $\pm 10\%$ of the initial value	Temperature: $-40, +125^\circ\text{C}$, Keeping 30 minutes Cycle:100 cycles Measurement : After placing for 24 hours min.
Low temperature storage	IEC61051-1	Appearance:Cracking,chipping or any other defects harmful to the characteristics shall not be allowed Vb:Within $\pm 10\%$ of the initial value	Temperature: $-40 \pm 5^\circ\text{C}$ Testing time:1000 \pm 24hours MeasurementAfter placing for 24 hours min.
High temperature storage	IEC61051-1	Appearance:Cracking,chipping or any other defects harmful to the characteristics shall not be allowed Vb:Within $\pm 10\%$ of the initial value	Temperature:125 \pm 5 $^\circ\text{C}$ Testing time:1000 \pm 24hours MeasurementAfter placing for 24 hours min.
Max. Energy	Specification Standard	Appearance:ceramic chip shall not be damaged. Vb:Within $\pm 10\%$ of the initial value	10/1000usWaveform, W_{max} , 1 surge current
ESD test	IEC61000-4-2	Appearance:ceramic chip shall not be damaged. Vb:Within $\pm 50\%$ of the initial value (For MLV- P/C/E/JES application test only)	Discharge:Air discharge Voltage:15kV Polarity: +, - Number:10 times in 10 seconds. Discharge: Contact discharge Voltage:8kV Polarity: +, - Number:10 times in 10 seconds.

Carrier Tape Specifications



Dimensions of Embossed Tape

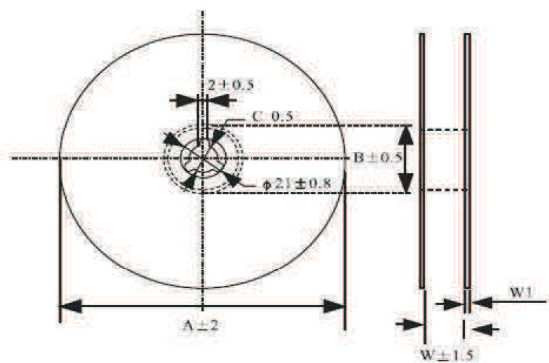
Size	$A_0 \pm 0.1$ (mm)	$B_0 \pm 0.1$ (mm)	$P_1 \pm 0.1$ (mm)	t_1/t_2 (mm)	t_3/t_4 (mm)	Quantity/Reel(Pcs)	
						Paper Tape	Embossed Tape
0402	0.62	1.10	2	—	1.0max/ 1.1max	10000	—
0603	1.08	1.88	4	—	1.0max/ 1.1max	4000	—
0805	1.42	2.30	4	0.6max/2.0max	1.0max/ 1.1max	4000	4000
1206	1.88	3.50	4	0.6max/2.9max	—	—	3000
1210	2.18	3.46	4	0.6max/2.9max	—	—	2000
1812	3.66	4.95	8	0.6max/2.9max	—	—	1000
2220	5.10	5.97	8	0.6max/2.9max	—	—	1000

A_0 : Width of Cavity
 B_0 : Length of Cavity
 P_1 : Pitch

t_1 : Embossed Tape Thickness
 t_2 : Height of Embossed Tape

t_3 : Paper Tape for Width
 t_4 : Paper Tape Bottom Width

Reel Specifications

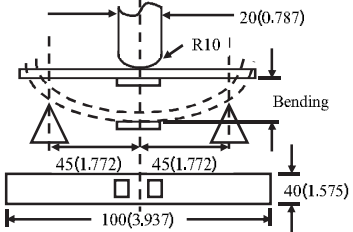
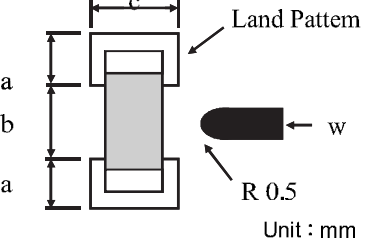
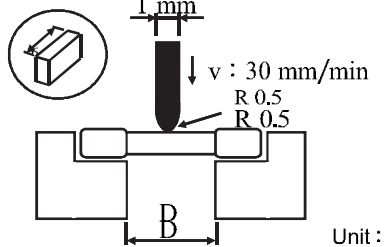
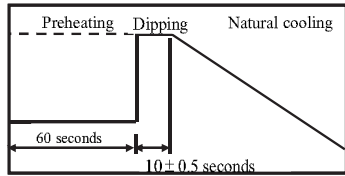
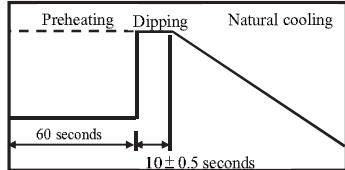


Dimensions

Size	A	B	C	W	1W
0402	178	60	13	10	1.6
0603	178	60	13	10	1.6
0805	178	60	13	10	1.6
1206	178	60	13	10	1.6
1210	178	60	13	10	1.6
1812	178	60	13.5	13.6	1.6
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Resistance to solder heat	IEC60068-2-20	The ceramic chip shall not be damaged. Shall be covered with solder. Vb: Within ±10% of the initial value.	Preheat:100°C~150°C,60seconds Solder temperature:260±5°C Dip time:10±1 seconds 																																								
Solderability	IEC60068-2-58	More than 90% of terminal electrode shall be covered with solder.	Preheat:100°C~150°C,60seconds Solder temperature:245±3°C Dip time:3±0.3seconds 																																								

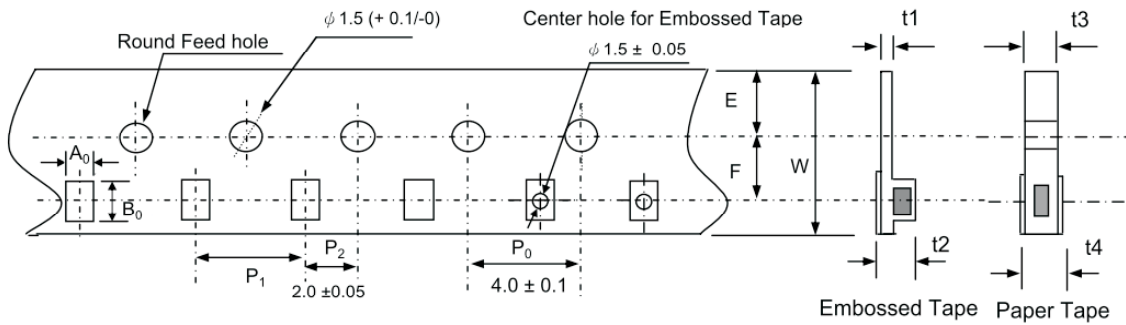
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Metal Oxide Varistor

■ Reliability-Multilayer Chip Varistor

Test description	Standard	Performance	Test condition
High temperature Load	IEC61051-1	Appearance:ceramic chip shall not be damaged. Vb:Within $\pm 10\%$ of the initial value	Temperature: $85 \pm 2^\circ\text{C}$ Testing time: 1000 ± 24 hours Load Voltage: Working voltage Measurement : After placing for 24 hours min.
Damp Heat Load, Steady State	IEC60068-2-78	Appearance:ceramic chip shall not be damaged. Vb:Within $\pm 10\%$ of the initial value	Humidity: 90 to 95% RH Temperature: $40 \pm 2^\circ\text{C}$ Testing time: 500 ± 24 hours at V_{DC} Measurement : After placing for 24 hours min.
Rapid Change of Temperature	IEC61051-1	Appearance:Cracking, chipping or any other defects harmful to the characteristics shall not be allowed Vb:Within $\pm 10\%$ of the initial value	Temperature: $-40, +125^\circ\text{C}$, Keeping 30 minutes Cycle: 100 cycles Measurement : After placing for 24 hours min.
Low temperature storage	IEC61051-1	Appearance:Cracking, chipping or any other defects harmful to the characteristics shall not be allowed Vb:Within $\pm 10\%$ of the initial value	Temperature: $-40 \pm 5^\circ\text{C}$ Testing time: 1000 ± 24 hours Measurement: After placing for 24 hours min.
High temperature storage	IEC61051-1	Appearance:Cracking, chipping or any other defects harmful to the characteristics shall not be allowed Vb:Within $\pm 10\%$ of the initial value	Temperature: $125 \pm 5^\circ\text{C}$ Testing time: 1000 ± 24 hours Measurement: After placing for 24 hours min.
Max. Energy	Specification Standard	Appearance:ceramic chip shall not be damaged. Vb:Within $\pm 10\%$ of the initial value	10/1000us Waveform, W_{max} , 1 surge current
ESD test	IEC61000-4-2	Appearance:ceramic chip shall not be damaged. Vb:Within $\pm 50\%$ of the initial value (For MLV- P/C/E/JES application test only)	Discharge: Air discharge Voltage: 15kV Polarity: +, - Number: 10 times in 10 seconds. Discharge: Contact discharge Voltage: 8kV Polarity: +, - Number: 10 times in 10 seconds.

Carrier Tape Specifications



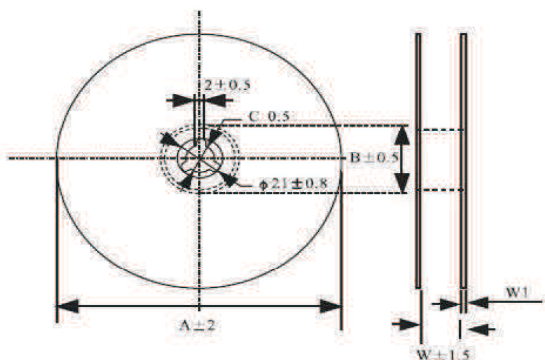
Dimensions of Embossed Tape

Size	$A_0 \pm 0.1$ (mm)	$B_0 \pm 0.1$ (mm)	$P_1 \pm 0.1$ (mm)	t_1/t_2 (mm)	t_3/t_4 (mm)	Quantity/Reel(Pcs)	
						Paper Tape	Embossed Tape
0402	0.62	1.10	2	—	1.0max/ 1.1max	10000	—
0603	1.08	1.88	4	—	1.0max/ 1.1max	4000	—
0805	1.42	2.30	4	0.6max/2.0max	1.0max/ 1.1max	4000	4000
1206	1.88	3.50	4	0.6max/2.9max	—	—	3000
1210	2.18	3.46	4	0.6max/2.9max	—	—	2000
1812	3.66	4.95	8	0.6max/2.9max	—	—	1000
2220	5.10	5.97	8	0.6max/2.9max	—	—	1000

A_0 : Width of Cavity
 B_0 : Length of Cavity
 P_1 : Pitch

t_1 : Embossed Tape Thickness
 t_2 : Height of Embossed Tape
 t_3 : Paper Tape for Width
 t_4 : Paper Tape Bottom Width

Reel Specifications



Dimensions

mm

Size	A	B	C	W	1W
0402	178	60	13	10	1.6
0603	178	60	13	10	1.6
0805	178	60	13	10	1.6
1206	178	60	13	10	1.6
1210	178	60	13	10	1.6
1812	178	60	13.5	13.6	1.6
2220	178	60	13.5	13.6	1.6

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